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A: It is a 32 bit word document. Can be opened in 32 bit office on 64 bit windows. File size -> size of file is 6.2 MB The present invention relates to semiconductor memory devices and, in particular, to a semiconductor memory device that includes a plurality of storage portions and a plurality of sense amplifiers, which are arranged around the storage portions. The present invention is related to Japanese patent application No. 11-159545, filed on May 20, 1999, No. 11-203877, filed on Jul. 7, 1999, and No. 11-231439, filed on Sep. 16, 1999. The contents of these applications are incorporated herein by reference. FIG. 1 shows a partial circuit diagram of a conventional semiconductor memory device in which each of N storage portions 1 is arranged along a memory row, and a corresponding sense amplifier 3 is arranged for every storage portion 1. The sense amplifiers 3 are arranged adjacent to the respective storage portions 1. The sense amplifiers 3 are connected to an X decoder 4, an Y decoder 5, and an I/O circuit 6. A latch circuit 7 is arranged in the I/O circuit 6, and the latch circuit 7 sequentially latches an input data signal DQA of bit A.sub.1 (1-bit) to bit A.sub.N, and outputs latched data to a global I/O line GIO of a number N+1. The X decoder 4 receives a row address signal ADD, and generates decoded signals X.sub.0 to X.sub.N. The Y decoder 5 receives the output signals of the X decoder 4 and an address signal ADD, and generates decoded signals X.sub.0 to Y.sub.N. The I/O circuit 6 receives the output signals of the X decoder 5, and a control signal, and controls the input/output timing of data. The operation of the semiconductor memory device is described below. The sense amplifiers 3 are arranged along the memory row, and the latch circuit 7 is arranged in the I/O circuit 6. Therefore, one sense amplifier 3 is arranged in correspondence to one memory cell, and the I/O circuit 6 is arranged in correspondence to the memory cell. When data is to be read out of a cell, for example, to read data of bit

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